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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726,188	11/29/2000	Jari A. Parviainen	872.0025USU	5987

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,188	PARVIAINEN, JARI A.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 06/14/2004.

2. Claims 1-24 are pending in this application. Claims 1, 10, and 21 are independent claims. This office action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 4, 7-8, 10-11, 13, 16-17, 20-21 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Abdallah et al. (U.S. 6,377,970).

Re claim 1, Abdallah et al. disclose in Figures 11-12 a data processor comprising: a multiplier block (Figure 12) having a multiplier front end (1100) for generating partial products from input operands (1140 and 1141), and a plurality of arithmetic logic units (1120 and 1110) having inputs switchably coupled (CNTR2 is deasserted), in a first mode of operation (multiplication as cited in col. 9 lines 28-35), to first data sources comprised of outputs of multiplier front end for adding together partial products received therefrom to arrive at a multiplication result (col. 9 line 39), inputs of plurality of ALUs being switchably coupled (CNTR2 is asserted), in a second mode of operation (e.g. performing

PADDH), to second data sources for performing at least one of arithmetic and logical operations on data received from second data sources (col. 10 lines 10-15).

Re claims 2 and 4, Abdallah et al. further disclose in Figure 12 partial products have a width of n-bits, and where a width of ALUs is one of n-bits or less than n-bits (col. 11 lines 14-16 wherein n = 16) wherein n = 16 bits (col. 9 lines 42-45).

Re claim 7, Abdallah et al. further disclose in Figure 1 inputs of ALUs are switchably coupled under control of a program instruction (CNTR2).

Re claim 8, Abdallah et al. further disclose in Figures 11-12 plurality of ALUs, when in the second mode of operation, operate in parallel with one another on data received from second data sources (1141).

Re claim 10, it is a method claim of claim 1. Thus, claim 10 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 11, it is a method claim of claim 2. Thus, claim 11 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 13, it is a method claim of claim 4. Thus, claim 13 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 16, it is a method claim of claim 7. Thus, claim 16 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 17, it is a method claim of claim 8. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 20, Abdallah et al. further disclose a reconfigurable signal routing logic (CNTR2) for providing data paths to and from plurality of ALUs.

Re claim 21, it is a DSP claim of claim 2. Thus, claim 21 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 24, it is a DSP claim of claim 20. Thus, claim 24 is also rejected under the same rationale in the rejection of rejected claim 20.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3, 5, 12, 14, 19 and 23 are rejected under 35 U.S.C. 103(a) as being obvious over Abdallah et al. (U.S. 6,377,970), as applied to claim 1 above, in view of Cheung et al. (U.S. 6,369,610).

Re claims 3 and 5, Abdallah et al. do not disclose implicitly partial products have a width of 8-bits/32-bits, and where a width of ALUs is one of 8-bits or 4-bits; and 32-bits, 16-bits, 8-bits or 4-bits respectively. However, Cheung et al. disclose in Figure 6 a multiplier comprising a basic block of 4-bit ALU (Figure 6). In addition, 8-bit ALUs and 32-bit ALUs are multiple of 4-bit ALU. Therefore, it would have been obvious application to a person having ordinary skill in the art at the time the invention is made to add 4-bit ALUs as a basic function block into a multiplier as seen in Cheung et al.'s invention into Abdallah et al.'s invention because it would enable to reduce the circuitry and simplify the complexity of multiplication hardware.

Re claims 12 and 14, they are method claim of claims 3 and 5 respectively. Thus, claims 12 and 14 are also rejected under the same rationale in the rejection of rejected claims 3 and 5 respectfully.

Re claim 19, Abdallah et al. do not disclose implicitly a plurality of ALUs comprise the same or additional ALUs that are coupled to inputs of multiplier front end for changing a sign of input operands. However, Cheung et al. disclose in Figure 4 that the operation of a multiplier of unsigned operands uses 2's complement for changing a sign of input operands (invert all bits +1). Therefore, it would have been obvious application to a person having ordinary skill in the art at the time the invention is made to change a sign of input operands as seen in Cheung et al.'s invention into Abdallah et al.'s invention because it would enable the multiplier system to perform in signed operands.

Re claim 23, it is a DSP claim of claim 19. Thus, claim 23 is also rejected under the same rationale in the rejection of rejected claim 19.

7. Claims 6, 9, 15, 18 and 22 are rejected under 35 U.S.C. 103(a) as being obvious over Abdallah et al. (U.S. 6,377,970), as applied to claim 1 above, in view of Aldrich et al. (U.S. 6,601,077).

Re claim 6, Abdallah et al. do not disclose partial products have a width of n-bits, where a width of ALUs is less than n-bits, and where at least some of plurality of ALUs are switchably coupled together to provide an n-bit wide ALU. However, Aldrich et al. disclose in Figure 3 an ALU (165) composes of several small ALUs (378 and 380) and coupled together to provide an n-bit wide ALU (165). Therefore, it would have been

obvious to a person having ordinary skill in the art at the time the invention is made to add a plurality of ALUs coupled together to form an ALU of n-bit wide as seen in Aldrich et al.'s invention into Abdallah et al.'s invention because it would enable to reduce the hardware complexity and handle efficiently any size of data (col. 2 lines 1-3 and col. 2 lines 35-40).

Re claim 9, Abdallah et al. do not disclose data processor forms a part of a wireless terminal. However, Aldrich et al. disclose in column 1 lines 15-18 the data processor forms a part of a wireless terminal (col. 1 line 17). Therefore, it would have been obvious application to a person having ordinary skill in the art at the time the invention is made to add the data processor into a wireless terminal as seen in Aldrich et al.'s invention into Abdallah et al.'s invention because it would enable to reduce the hardware, reduce the cost of implement, and increase the reliability in DSP in wireless communication (col. 1 lines 15-22).

Re claim 15, it is a method claim of claim 6. Thus, claim 15 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 18, it is a method claim of claim 9. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 22, it is a DSP claim of claim 9. Thus, claim 22 is also rejected under the same rationale in the rejection of rejected claim 9.

Response to Arguments

8. Applicant's arguments filed 06/14/2004 have been fully considered but they are not persuasive.

a. The applicant argues in pages 2-3 for independent claims that Abdallah et al. do not disclose or suggest any first mode of operation where first data sources are comprised of outputs of a multiplier front end for adding together partial products received therefrom to arrive at a multiplication result, and a second mode of operation performing at least one of arithmetic and logical operations on data received from said second data source.

The examiner respectfully submits that the previous office action clearly points out the rejection by Abdallah et al. reference of all the limitations cited the claims. In particular, the first mode is used to process the PMAD instruction (packed multiply-add instruction) which is similar to the MAC instruction (multiply-accumulated instruction). The PMAD instruction is activated when a control signal (CNTR2) is deasserted which generates partial products from sources and sum up all the partial products to yield a final product. The second mode is used to process the PADDH instruction (packed add-horizontal instruction). The PADDH instruction is activated when the same control is asserted which reconfigure to add a set of source data using the same multiplier as above. Therefore based on the claim language, Abdallah et al. clearly disclose or suggest a first mode of operation (PMAD instruction/mode when CNTR2 is deasserted) where first data sources (outputs of the partial product generator) are comprised of

outputs of a multiplier front end for adding together partial products received therefrom to arrive at a multiplication result (output of the PMAD instruction as seen in Figure 5 register R), and a second mode of operation (PADDH instruction/mode when CNTR2 is asserted) performing at least one of arithmetic and logical operations on data (horizontally add the received data) received from said second data source (data input into 1140 in Figure 11).

b. The applicant comments in page 5 second paragraph for independent claims that the advantage of aspects of the presently claimed invention is in providing a DSP wherein a multiplier front end comprises at least one configurable ALU, where the ALU is employed for accumulating partial results during MAC operations (multiplication results) and may also be used as one or more ALUs during non-MAC operations (arithmetic and/or logical operations). According to aspects of the claimed invention, the ALUs inputs are switch ably or programmable coupled. In a first mode, the ALUs inputs are coupled to first data sources and in the second mode ALUs inputs are coupled to second data sources. A further advantage is that the plurality of ALUS can operate together in parallel.

The examiner respectfully submits that the claim language does not clearly cited the above limitations or unique advantages wherein the first mode is used for MAC operation and the second is used for non-MAC operation and further the ALUs can be operate together in parallel.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

August 17, 2004

TODD INGBERG
PRIMARY EXAMINER